EE 673, Power Electronics and Power System Laboratory

Indian Institute of Technology, Bombay

Experiment – 04: Double Pulse Test of SiC MOSFET

Handout - Activity

Date- ***Duration: 3 hours***

LTspice: (1.5 hours)

Activity 01: Import the SPICE model for the MOSFET with part number **C3M0060065K** into LTSpice and create a schematic for a **double pulse test** circuit using this switch. Ensure the schematic includes the following parasitic elements:

- Parasitic inductance at the DC bus.
- Parasitic inductances at the drain, source, and gate terminals of the MOSFETs.

Activity 02: Configure the proper gate drive pulses for the double pulse test circuit created in **Activity 01** using piece wise linear voltage source**.**

Activity 03: Run the circuit and explain the following to your TA

- Slope change and ringing in drain to source voltage of the device under test (DUT) during turn-on and turn-off transitions
- Plateau in the gate to source (Kelvin source) voltage of the DUT.
- Overshoot and ringing in the drain current of the DUT during turn on transition.

Activity 04 - Calculate the following using waveforms obtained: t_{on}, t_{off}, E_{on}, E_{off}

Activity 05- Now Connect the gate driver between the gate (G) and source (S) pins instead of the gate (G) and Kelvin source (K) pin of the DUT. Observe and explain the changes in the gate-to-source voltage, as well as the effects on t_{on}, t_{off}, E_{on}, E_{off}

Activity 06- Introduce a decoupling capacitor across the DC- link and explain its effect on the switching characteristics of the DUT.

Activity 07- Connect a capacitor across drain and source of the DUT and explain its effect on different switching waveforms to your TA.

Activity 08- Run the circuit for four different values of gate resistance. Explain how gate resistance affects the switching characteristics of the DUT to your TA.

Hardware: (1.5 hours)

Activity 01: Check the pulses obtained from the microcontroller using the DSO and ensure they match the expected output.

Activity 02: Verify the gate pulses of the DUT without powering the DC bus.

Activity 03: Turn on the DC-link voltage and run the microcontroller code to perform the double pulse test.

Activity 04: Examine the alignment of switching waveforms. If misaligned, perform de-skewing using the DSO and repeat the test to confirm alignment.

Activity 05: Observe the switching waveforms: v_{DS}, v_{GS}, i_D and explain their behaviour to your TA.

Activity 06: Measure the switching times (t_{on}, t_{off}) from the obtained waveforms using the DSO.

Activity 07:

- Use the math function of the DSO to calculate the instantaneous switching power loss (p_s) waveform.
- Determine E_{on}, E_{off} from the instantaneous power loss waveform.
- Capture and save the waveforms (v_{DS}, v_{GS}, i_D, p_s) as snapshots.
- Export the waveform data in .csv format.

Activity 08: Replace the gate resistance with a different value and repeat Activity 01 to Activity 07 for comparative analysis.

Post-lab Activity:

- Write a MATLAB or Python script to analytically calculate the switching energy loss of the DUT (C3M0060065K). Ensure the script is well commented for easy understanding.
- Provide a detailed explanation of the switching waveforms (v_{DS}, v_{GS}, i_D, p_s) through either a power point presentation or a video narration. Highlight key features and transitions during the switching process.
- Compare the energy loss measurements (E_{on}, E_{off}) obtained from three methods:
    - LTspice simulation
    - Hardware results
    - Analytical calculation

For a specific gate resistance value, explain the differences and their possible causes.

- Use the saved waveform data (.csv format) to plot v_{DS}, v_{GS}, i_D, p_s on the same time axis for different gate resistance values.
    - Explain how varying gate resistance affects the switching waveforms.
    - Highlight the trade-offs involved in choosing gate resistance values.